CLAIMS

1. (cancelled) A method of making an electrode on a semiconductor structure, comprising:

a) depositing metal on a surface of a semiconductor structure;

b) forming a patterned mask over the metal on the semiconductor structure, the mask having at least one opening so that a first region is covered by the mask and a second region aligned with the at least one opening is left uncovered by the mask;

c) removing metal aligned with the at least one opening in the second region, so as to reveal the top surface of the semiconductor structure in the second region; and

d) removing material of the semiconductor structure aligned with the at least one opening in the second region.

2. (cancelled) The method of claim 1, wherein the metal comprises a first metal and a second metal.

3. (cancelled) The method of claim 2, wherein said first metal and second metal are selected to form a substantially transparent material upon annealing.

4. (cancelled) The method of claim 3, further comprising annealing the first metal and second metal.

5. (cancelled) The method of claim 4, wherein the first metal comprises nickel and the second metal comprises gold.

6. (cancelled) The method of claim 2, wherein the step of depositing comprises electron beam deposition.

7. (cancelled) The method of claim 6, wherein the step of depositing metal comprises depositing a first metal and depositing a second metal overlying the first metal.

8. (cancelled) The method of claim 1, wherein the step of forming a patterned mask comprises applying a resist on the metal and lithographically patterning the resist to form the at least one opening over the second region so that the remaining resist overlies the semiconductor structure in the first region.

9. (cancelled) The method of claim 8, wherein the step of removing metal comprises etching.

10. (cancelled) The method of claim 9, wherein the step of etching comprises etching with KI:I2:DI solution.

11. (cancelled) The method of claim 9, wherein the step of removing material from the semiconductor structure comprises etching the semiconductor structure while the resist remains over the semiconductor structure in the first region.

12. (cancelled) The method of claim 10, wherein the step of removing material from the semiconductor structure comprises a reactive ion etching.

13. (cancelled) The method of claim 12, wherein the step of etching comprises etching with BCl_3.

14. (cancelled) The method of claim 8, wherein the resist layer covering the first region has edges and the step of removing metal is performed so as to remove some of the metal underneath the resist layer adjacent the edges of the resist layer to form a space between the edges of the resist layer and the metal on the semiconductor structure.

15. (cancelled) The method of claim 14, wherein the metal in the first region substantially covers the first region except in said space.

16. (cancelled) The method of claim 1, wherein the step of removing material from the semiconductor structure in the second region is performed so as to leave the first region protruding from the remainder of semiconductor structure.

17. (cancelled) The method of claim 16, wherein the semiconductor structure comprises a p-type semiconductor layer overlying an n-type semiconductor layer arranged beneath the p-type semiconductor layer, the semiconductor structure having a junction between the p-type layer and the n-type layer.

18. (cancelled) The method of claim 17, wherein, after material is removed from the semiconductor structure in the second region, an upwardly protruding portion comprising the p-type layer and a lower region comprising a portion of the n-type layer are formed.

19. (cancelled) The method of claim 17, wherein the metal covers a large portion of the semiconductor structure in the first region, the metal being in contact with the p-type layer.

20. (cancelled) The method of claim 18, further comprising forming a lower electrode on the n-type layer of the second region.

21. (withdrawn) A method of making a transparent electrode for light-emitting diode, comprising:

a) depositing metal on a top surface of a semiconductor structure;

b) defining a first region of the semiconductor structure for a first electrode by forming a mask over the metal, the mask having at least one opening so that the

first region is covered by the mask and a second region is aligned with the at least one opening in the mask;

c) removing metal aligned with the at least one opening in the mask in the second region so as to reveal the top surface of the semiconductor structure in the second region; and

d) removing material from the semiconductor structure aligned with the at least one opening in the second region to form a second electrode surface for a second electrode, the second electrode surface being lower in elevation than the top surface of the semiconductor structure.

22. (withdrawn) The method of claim 21, wherein the step of depositing metal includes depositing a first metal and depositing a second metal.

23. (withdrawn) The method of claim 22, further comprising annealing the first metal and second metal.

24. (withdrawn) The method of claim 22, wherein said first metal and second metal are selected to form a substantially transparent material upon annealing.

25. (withdrawn) The method of claim 22, wherein the first metal comprises nickel and the second metal comprises gold.

26. (withdrawn) The method of claim 21, wherein the step of depositing comprises electron beam deposition.

27. (withdrawn) The method of claim 23, wherein the step of depositing metal comprises depositing a first metal and depositing a second metal overlying the first metal.

28. (withdrawn) The method of claim 21, wherein the step of defining a first region comprises applying a resist on the metal, and lithographically patterning the resist to form at least one opening in the second region so that the remaining resist overlies the semiconductor structure in the first region.

29. (withdrawn) The method of claim 21, wherein the step of removing metal comprises etching.

30. (withdrawn) The method of claim 29, wherein the step of etching comprises etching with KI:I2:DI solution.

31. (withdrawn) The method of claim 29, wherein the step of removing material from the semiconductor structure comprises etching the semiconductor structure while the resist remains in the first region.

32. (withdrawn) The method of claim 31, wherein the step of removing material from the semiconductor structure comprises reactive ion etching.

33. (withdrawn) The method of claim 31, wherein the step of etching comprises etching with BCl_3.

34. (withdrawn) The method of claim 28, wherein the resist layer in the first region has edges and the step of removing metal is performed so as to remove some of the metal underneath the resist layer adjacent the edges of the resist layer to form a space between the edges of the resist layer and the metal on the semiconductor structure.

35. (withdrawn) The method of claim 34, wherein the metal in the first region substantially covers the first region except in said space.

36. (withdrawn) The method of claim 21, wherein the step of removing material from the semiconductor structure in the second region is performed so as to leave the first region protruding from the remainder of semiconductor structure.

37. (withdrawn) The method of claim 36, wherein the semiconductor structure comprises a p-type semiconductor layer overlying an n-type semiconductor layer arranged beneath the p-type semiconductor layer, the semiconductor structure having a junction between the p-type layer and the n-type layer.

38. (withdrawn) The method of claim 37, wherein the first region comprises an upwardly protruding portion of the p-type layer and the second region comprises a portion of the n-type layer.

39. (withdrawn) The method of claim 38, wherein the first region forms the mesa of the light-emitting diode, and the metal forms an electrode on the mesa.

40. (withdrawn) The method of claim 37, wherein the metal covers a large portion of the semiconductor structure in the first region, the metal being in contact with the p-type layer.

41. (withdrawn) The method of claim 37, further comprising forming a lower electrode on the n-type layer of the second region.

42. (new) A method of forming electrodes on first and second respective regions of a semiconductor structure, comprising:

a) depositing metal on a surface of a first region of the semiconductor structure;

b) forming a patterned mask over the metal on the surface of the first region, the mask having an opening so that a first portion is covered by the mask and a second portion aligned with the opening is left uncovered by the mask;

c) removing metal aligned with the opening in the second portion thereby defining a first electrode overlying and making electrical contact with the first region of the semiconductor structure;

d) removing material of the semiconductor structure aligned with the opening in the second portion to expose a surface of the second region of the semiconductor structure; and

e) forming a second electrode making electrical contact with the second region of the semiconductor structure.

43. (new) The method of claim 42, wherein the step of depositing metal comprises depositing a first metal and subsequently depositing a second metal over the first metal.

44. (new) The method of claim 43, wherein the first metal comprises nickel and the second metal comprises gold, and further comprising annealing the structure so that the metal layers form a substantially transparent material.

45. (new) The method of claim 42, wherein the step of depositing comprises electron beam deposition.

46. (new) The method of claim 42, wherein the step of forming a patterned mask comprises applying a resist on the metal to form a resist layer, and lithographically patterning the resist layer to form the at least one opening over the second region so that the remaining resist layer overlies the semiconductor structure in the first region.

47. (new) The method of claim 42, wherein the step of removing metal comprises etching.

48. (new) The method of claim 42, wherein the step of etching comprises etching with KI:I2:DI solution.

49. (new) The method of claim 46, wherein the step of removing material from the semiconductor structure comprises etching the semiconductor structure while the resist layer remains over the semiconductor structure in the first region.

50. (new) The method of claim 42, wherein the step of removing material from the semiconductor structure comprises a reactive ion etching.

51. (new) The method of claim 42, wherein the step of etching comprises etching with BCl_3.

52. (new) The method of claim 49, wherein the resist layer covering the first region has an edge circumscribing the opening and the step of removing metal removes some of the metal underneath the resist layer adjacent the edge of the resist layer to form a gap between the edge of the resist layer and the metal on the semiconductor structure.

53. (new) The method of claim 52, wherein the metal in the first region substantially covers the first region except in said gap.

53. (new) The method of claim 49, wherein the step of removing material from the semiconductor structure in the second region is performed so as to leave the first region protruding from the remainder of semiconductor structure.

54. (new) The method of claim 42, wherein the first region of the semiconductor structure includes a p-type semiconductor layer, and the second region includes an n-type semiconductor layer arranged beneath the p-type semiconductor layer, the semiconductor structure having a junction between the p-type layer and the n-type layer.

55. (new) The method of claim 54, wherein, after material is removed from the semiconductor structure in the second region, an upwardly protruding portion comprising the p-type layer and a lower region comprising a portion of the n-type layer are formed.

56. (new) The method of claim 54, wherein the metal covers a large portion of the semiconductor structure in the first region, the metal being in contact with the p-type layer.

57. (new) The method of claim 54, wherein the step of forming a second electrode includes depositing metal to make electrical contact with the n-type layer of the second region.